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UTILITY PATENT APPLICATION TRANSMITTAL

Attorney Docket No. Total Pages MI22-1098 First Named Inventor or Application Identifier

Klaus F. Schuegraf

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application	on contents.	Assistant Commissioner for Patents ADDRESS TO: Box Patent Application Washington, DC 20231					
1. X Fee Transmittal Form (Submit an original, and a duplicate for fee pro 2. X Specification [Total Page (preferred arrangement set forth below) - Descriptive title of the Invention + CO - Cross References to Related Application - Statement Regarding Fed sponsored F	es 26] over sheet	Microfiche Computer Program (Appendix) Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. Computer Readable Copy b. Paper Copy (identical to computer copy)					
 Reference to Microfiche Appendix Background of the Invention 		c. Statement verifying identity of above copies					
 Brief Summary of the Invention Brief Description of the Drawings (if file) 	d)	ACCOMPANYING APPLICATION PARTS					
- Detailed Description - Claim(s) - Abstract of the Disclosure 3.	es 3] or CFR 1.63(d)) or CFR 1.63(d)) or completed) or completed) or completed) or completed) or application, or application	(if foreign priority is claimed) 16. X Other: Check for \$838.00 Substitute Drawing Request					
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18. CORRESPONDENCE ADDRESS Customer Number or Bar Code Label O21567 or Correspondence address below (Insert Customer No. or Attach, bar code label fiere)							
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FEE TRANSMITTAL

Note: Effective October 1, 1997. Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT (\$) 838.00

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Complete if Known			
Application Number	PRIORITY 08/696,243		
Filing Date	PRIORITY Aug. 13, 1996		
First Named Inventor	Klaus F. Schuegraf		
Group Art Unit	PRIORITY 2813		
Examiner Name	PRIORITY M. Whipple		
Attornov Dooket Number	IMI22-1098		

METHOD OF PAYMENT (check one)		F	EECALCULATION (continued)	
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Deposit Account Name Wells, St. John et al.	127 50	227 25	Surcharge - late provisional filing fee or cover sheet.	0
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Fee Required Under 37 CFR 1.18 at the Mailing of the Notice of Allowance	147 2,520	147 2,520	For filing a request for reexamination	0
	112 920*	112 920*	Requesting publication of SIR prior to Examiner action	0
2. X Payment Enclosed: X Check Order Other	113 1,840*	113 1,840	* Requesting publication of SIR after Examiner action	0
FEE CALCULATION	115 110	215 55	Extension for reply within first month	0
FEE CALCULATION	116 400	216 200	Extension for reply within second month	0
1. FILING FEE	117 950	217 475	Extension for reply within third month	0
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101 790 201 395 Utility filing fee 760	119 310	219 155	Notice of Appeal	0
106 330 206 165 Design filing fee	120 310	220 155	Filing a brief in support of an appeal	0
107 540 207 270 Plant filing fee	121 270	221 135	Request for oral hearing	0
108 790 208 395 Reissue filing fee	138 1,510	138 1,510	Petition to institute a public use proceeding	0
114 150 214 75 Provisional filing fee	140 110	240 55	Petition to revive - unavoidable	0
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2. CLAIMS Extra Fee from Fee Paid	143 450	243 225	Design issue fee	0
Total Claims 10 -20 = 0 X =	144 670	244 335	Plant issue fee	0
Independent	122 130	122 130	Petitions to the Commissioner	0
Multiple Dependent Claims X =	123 50	123 50	Petitions related to provisional applications	0
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103 22 203 11 Claims in excess of 20	146 790	246 395	Filing a submission after final rejection (37 CFR 1.129(a))	
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			examined (37 CFR 1.129(b))	l ol
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SUBMITTED BY	Y				 Complete (if	applicable)	
Typed or Printed Name	Lance R. Sadler		í	J	Reg. Number	38,605	
Signature	Jon Jan	Date	12/1	5/9	Deposit Account User ID		

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PriorityApplicationSerial No.08/696,243PriorityFiling Date08/13/96InventorSchuegrafAssigneeMicron Technology, Inc.PriorityGroup Art Unit2813PriorityExaminerM. WhippleAttorney's Docket No.MI22-1098Title:Semiconductor Processing Methods of Chemical Vapor Depositing SiO2 on
a Substrate

PRELIMINARY AMENDMENT

To: Box PATENT APPLICATION

Assistant Commissioner for Patents

Washington, D.C. 20231

From: Lance R. Sadler (Tel. 509-624-4276; Fax 509-838-3424)

Wells, St. John, Roberts, Gregory & Matkin P.S.

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Applicant preliminarily amends as follows:

<u>AMENDMENTS</u>

In the Specification

On page 1, before the "Technical Field" section, insert the following section:

--RELATED PATENT DATA

This patent resulted from a continuation application of U.S. Patent Application Serial No. 08/696,243, filed August 13, 1996, entitled "Semiconductor Processing Methods of Chemical Vapor Depositing SiO₂

on a Substrate", naming Klaus F. Schuegraf as inventor, and which is now U.S. Patent No. _____ the disclosure of which is incorporated by reference.--

In the Claims

Cancel claims 1-38 without prejudice.

New Claims

Add new claims 39-48 as follows:

39. A semiconductor processing method of depositing SiO_2 on a substrate within a chemical vapor deposition reactor comprising feeding at least one of H_2O and H_2O_2 into the reactor while feeding an organic silicon precursor, wherein the at least one of H_2O and H_2O_2 is fed into the reactor separately from the organic silicon precursor, and under conditions which are effective to reduce the decomposition rate of the organic silicon precursor.

40. The semiconductor processing method of claim 39, wherein the at least one of H_2O and H_2O_2 comprises less than about 50% by volume of material injected into the reactor.

- 41. The semiconductor processing method of claim 40, wherein the at least one of H_2O and H_2O_2 comprises between about 5% to 15% by volume of material injected into the reactor.
- 42. The semiconductor processing method of claim 40, wherein the at least one of H_2O and H_2O_2 comprises less than about 5% by volume of material injected into the reactor.
- 43. A semiconductor processing method of forming silicon dioxide comprising feeding at least one of H_2O and H_2O_2 into a chemical vapor deposition reactor with an organic silicon precursor under conditions effective to decompose the organic silicon precursor into silicon dioxide and reduce formation of undesired reaction intermediates in the reactor during the decomposition reaction, wherein the at least one of H_2O and H_2O_2 is fed into the reactor separately from the organic silicon precursor, said organic silicon precursor being the only silicon containing precursor which is fed into the reactor to form said silicon dioxide.
- 44. The semiconductor processing method of claim 43, wherein the organic silicon precursor is selected from the group consisting of: silane, tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclotetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).

45. The semiconductor processing method of claim 43, wherein the chemical vapor deposition reactor is a hot wall reactor.

- 46. The semiconductor processing method of claim 43, wherein the chemical vapor deposition reactor is a cold hot reactor.
- 47. A semiconductor processing method of chemical vapor depositing SiO₂ on a substrate comprising:

placing a substrate within a chemical vapor deposition reactor;

feeding an organic silicon precursor into the chemical vapor deposition reactor having the substrate positioned therein under conditions effective to decompose the precursor into SiO₂ which deposits on the substrate and into a gaseous oxide of hydrogen; and

feeding an additional quantity of the gaseous oxide of hydrogen into the reactor while feeding the organic silicon precursor into the reactor, wherein the organic silicon precursor and the additional quantity of the gaseous oxide of hydrogen are fed into the reactor from separate feed streams and under conditions which are effective to reduce the decomposition rate of the organic silicon precursor into the SiO₂.

48. A semiconductor processing method of chemical vapor depositing SiO₂ on a substrate comprising:

placing a substrate within a hot wall low pressure chemical vapor deposition reactor;

feeding an organic silicon precursor into the hot wall chemical vapor deposition reactor having the substrate positioned therein under conditions effective to decompose the precursor into SiO₂ which deposits on the substrate and into a gaseous oxide of hydrogen; and

feeding an additional quantity of the gaseous oxide of hydrogen into the hot wall low pressure chemical vapor deposition reactor while feeding the organic silicon precursor into the reactor, wherein the organic silicon precursor and the additional quantity of the gaseous oxide of hydrogen are fed into the reactor from separate feed streams.

REMARKS

Claims 1-38 have been canceled without prejudice. Claims 39-48 have been added and remain in the application for consideration.

Respectfully submitted,

Dated: 12/15/98

Lance R. Sadler Reg. No. 38,605

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

Semiconductor Processing Methods Of Chemical Vapor Depositing SiO₂ On A Substrate

INVENTOR

Klaus F. Schuegraf

ATTORNEY'S DOCKET NO. MI22-482

EL169836626 EM189770036

TECHNICAL FIELD

II

This invention relates to semiconductor processing methods of chemical vapor depositing SiO_2 on a substrate.

BACKGROUND OF THE INVENTION

Chemical vapor deposited (CVD) SiO₂ films and their binary and ternary silicates find wide use in VLSI processing. These materials find use as insulators between polysilicon and metal layers, between metal layers in multilevel metal systems, as diffusion sources, as diffusion and implantation masks, as capping layers to prevent outdiffusion, and as final passivation layers.

The manner in which a thin film covers or conforms to the underlying features on a substrate is an important characteristic in semiconductor processing. Conformal coverage refers to coverage in which equal film thickness exists over all substrate topography regardless of its slope, i.e. vertical and horizontal substrate surfaces are coated with equal film thickness.

One manner of effecting the deposition of SiO_2 on a substrate is through pyrolysis of an organic silicon precursor in a CVD reactor to form SiO_2 . A typical organic silicon precursor is tetraethoxysilane or TEOS which is represented by the chemical formula $Si(OC_2H_5)_4$. A typical reactor used to effect the pyrolysis of organic silicon precursors is a low pressure CVD reactor or LPCVD reactor. LPCVD

reactors include both hot wall and cold wall reactors. In hot wall reactors, wafers can be heated utilizing radiant heat supplied from resistance-heated coils. In cold wall reactors, wafers can be heated utilizing infrared lamps or rf induction.

LPCVD reactors are typically operated at pressures of around 0.25-2.0 Torr and temperatures of around 550° C to 800° C, although such parameters may vary depending on a number of different conditions including the particular types of reactants used. The stoichiometry of decomposition of TEOS within an LPCVD reactor may be simplistically written as:

$$Si(OC_2H_5)_4 ---> SiO_2 +4C_2H_4 + H_2O_2$$

Typically, however, intermediates are formed in the above reaction which include di-ethoxysilane $(Si(OC_2H_5)_3OH)$ and tri-ethoxysilane $(Si(OC_2H_5)_2(OH)_2)$. Further, other reaction by-products are formed.

One problem facing the semiconductor wafer processor is achieving adequate and conformal step coverage of deposited SiO₂ into very deep and narrow contact openings or other so-called high aspect ratio topographies. One such substrate surface topography is depicted in Figs. 1 and 2 and designated generally by reference numeral 10. Topography 10 is defined by a deep trench 12 into which an SiO₂ layer 14 has been deposited as by CVD of a suitable organic silicon precursor such as TEOS.

Fig. 1 illustrates a situation in which adequate conformality has been achieved as evidenced by the uniformity or substantial uniformity in thickness of layer 14 over the substrate surface, and particularly within trench 12. Fig. 2 illustrates a situation in which inadequate conformality has resulted in non-uniformity in the thickness of layer 14, particularly at and near the bottom of trench 12. Such is an undesirable condition.

One source of inadequate conformality of SiO_2 on a substrate surface is premature formation of undesirable intermediates which react to form SiO_2 at higher topographical elevations on a substrate surface. Consequently, such intermediates never reach the bottom of a particular substrate feature, such as trench 12 of Fig. 2, so that lesser degrees of SiO_2 are formed thereon.

One method to improve step coverage has been to increase pressures in the CVD reactor. By doing so, the partial pressure of the organic silicon precursor, such as TEOS, is increased, while the partial pressure of the intermediates is not. The increase in organic silicon precursor partial pressure results in improved step coverage because the precursor has a more favorable sticking coefficient as compared with the intermediates.

Another attempt to increase step coverage has been to introduce ethylene (C_2H_4) into the reactor with the precursor to inhibit the premature formation of intermediates. Unfortunately, great success has

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not been achieved due to significant degradation of deposition rates stemming from competitive absorption relative to the substrate surface as between the ethylene and the precursor.

This invention grew out of the need to provide improved step coverage of LPCVD SiO₂ over high aspect ratio substrate topography.

SUMMARY OF THE INVENTION

The invention provides semiconductor processing methods of depositing SiO_2 on a substrate.

In a preferred aspect, the invention provides methods of reducing the formation of undesired reaction intermediates in a chemical vapor deposition (CVD) decomposition reaction. In one implementation, the method is performed by feeding at least one of H_2O and H_2O_2 into a reactor with an organic silicon precursor. For example, in one exemplary implementation, such components are, in gaseous form, fed separately into the reactor. In another exemplary implementation, such components are combined in liquid form prior to introduction into the reactor, and thereafter rendered into a gaseous form for provision into the reactor. The invention can be practiced with or in both hot wall and cold wall CVD systems.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 illustrates a so-called high aspect ratio semiconductor topography in the form of a trench into which silicon dioxide has been deposited achieving adequate conformal coverage.

Fig. 2 illustrates a high aspect ratio semiconductor topography similar to Fig. 1, only one in which inadequate conformal coverage has been achieved.

Fig. 3 is a schematic diagram of a chemical vapor deposition system which may be used in conjunction with one preferred aspect of the invention.

Fig. 4 is a schematic diagram of a chemical vapor deposition system which may be used in conjunction with another preferred aspect of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the invention, a semiconductor processing method of chemical vapor depositing SiO₂ on a substrate comprises:

placing a substrate within a chemical vapor deposition reactor;

feeding an organic silicon precursor into the chemical vapor deposition reactor having the substrate positioned therein under conditions effective to decompose the precursor into SiO₂ which deposits on the substrate and into a gaseous oxide of hydrogen; and

feeding an additional quantity of the gaseous oxide of hydrogen into the reactor while feeding the organic silicon precursor to the reactor.

In accordance with another aspect of the invention, a semiconductor processing method of reducing the decomposition rate of an organic silicon precursor in a chemical vapor deposition process of depositing SiO_2 on a substrate within a chemical vapor deposition reactor comprises feeding at least one of H_2O and H_2O_2 into the reactor while feeding the organic silicon precursor.

In accordance with another aspect of the invention, a semiconductor processing method of chemical vapor depositing SiO₂ on a substrate comprises:

placing a substrate within a chemical vapor deposition reactor; and feeding an organic silicon precursor and feeding an oxide of hydrogen into the chemical vapor deposition reactor having the substrate positioned therein under conditions effective to deposit an SiO₂ layer on the substrate.

In accordance with another aspect of the invention, a semiconductor processing method of reducing the formation of undesired reaction intermediates in a chemical vapor deposition decomposition reaction of an organic silicon precursor into silicon dioxide within a chemical vapor deposition reactor comprises feeding at least one of $\rm H_2O$ and $\rm H_2O_2$ into the reactor with the organic silicon precursor.

Figs. 3 and 4 show schematic diagrams of a different chemical vapor deposition (CVD) systems both of which are designated at 16. The preferred semiconductor processing methods may be carried out in either system in accordance with the description below. The system of Fig. 3 is configured slightly differently from the system of Fig. 4 as will become apparent below. Preferably, CVD systems 16 are low pressure chemical vapor deposition (LPCVD) hot wall systems, although other CVD systems, such as cold wall systems can be used as will become apparent. The illustrated and preferred hot wall systems 16 include a

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CVD reactor 18 which is configured to carry out depositions at temperatures between around 640° C to 900° C, and at pressures between 100 mTorr to 3 Torr. Various gases can be supplied to reactor 18 from one or more gas sources or bubblers, such as those shown at 20. Such gas sources or bubblers typically hold or contain a liquid mixture which is heated to produce a gas. Such gas from gas sources 20 enters CVD reactor 18 where exposure to temperature and pressure conditions effect deposition of a material, preferably SiO₂, on a semiconductor or wafer substrate therewithin. More than one gas source (Fig. 4) may be used. Inside of CVD reactor 18, a semiconductor wafer holder 22 is provided for holding a plurality of semiconductor wafers or substrates 24. After suitable deposition has occurred, gaseous by-products are exhausted, together with unused reactant and/or diluent gases through exhaust port 26. Reactant gases may be carried by inert diluent or carrier gases such as H2, N2 or Ar.

Fig. 3 shows system 16 configured for carrying out one preferred semiconductor processing method of chemical vapor depositing SiO₂ on a substrate. Accordingly, system 16 includes a gas source 28. An example of a suitable gas source is a bubbler which contains liquid reactants which are subsequently converted into a gas for provision into a reactor, such as reactor 18. The illustrated and preferred method includes placing a substrate or substrates, such as those shown at 24, within a chemical vapor deposition reactor, such as reactor 18.

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Reactants which are held in gas source 28 are then heated to produce a gas which is supplied to reactor 18 for further processing in accordance this method. One such reactant is a suitable organic silicon precursor which is preferably tetraethoxysilane or TEOS. Such precursor is fed into reactor 18 wherein substrate 24 is positioned under processing conditions, such as the temperature and pressure conditions mentioned above, which are effective to decompose the precursor into SiO₂. Although the preferred methods are described as utilizing TEOS as the preferred organic silicon precursor, other such organic silicon precursors may be used. Other precursors include: silane, diethylsilane (TMCTS), fluorotriethoxysilane (DES), tetramethylcyclo-tetrasiloxane (FTES), and fluorotrialkoxysilane (FTAS). The SiO₂ deposits on substrates 24 and preferably into high-aspect topography features such as trench 12 in Fig. 1. The organic silicon precursor also decomposes into a gaseous oxide of hydrogen such as H₂O and H₂O₂. According to a preferred aspect of the invented method, another reactant, preferably either H₂O or H₂O₂, is provided in liquid form in gas source Such additional quantity of the oxide of hydrogen is fed into 28. reactor 18 in gaseous form, while feeding the organic silicon precursor The presence of the additional quantity of the into the reactor. gaseous oxide of hydrogen shifts the reaction equilibrium in the direction of the reactants, thus increasing the partial pressure of the organic silicon precursor. Such inhibits or reduces premature formation

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of undesirable intermediates which heretofore have reduced the conformality of the deposition process.

Referring still to Fig. 3, quantities of TEOS and the additional quantity of the oxide of hydrogen, both in liquid form, are mixed together to form a liquid mixture. The liquid mixture formed thereby is then converted to a gaseous mixture which is thereafter fed into reactor 18. By first combining liquid forms of the oxide of hydrogen and the organic silicon precursor, and then feeding the gaseous mixture produced thereafter into the reactor, the organic silicon precursor and the additional gaseous quantity of the oxide of hydrogen are fed into the reactor together. Preferably, the quantity of organic silicon precursor, in this example TEOS, in the liquid mixture is greater by volume than the quantity of the oxide of hydrogen. preferably, the liquid mixture volume comprises between about 5% to 15% of the oxide of hydrogen. Volumes of the oxide of hydrogen less than about 5% can be utilized to achieve the above-described advantages. Volumes of about 0.5% or lower of either of the oxides of hydrogen may also be utilized. Conversion of the liquid mixture to the gaseous mixture preferably takes place at bubbler temperatures between about 65° to 80°C with a preferred temperature of about 75°C. Thereafter, the gaseous mixture is fed into reactor 18 where it is reacted to deposit SiO₂ on substrates 24 therewithin.

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The above described method is one in which the organic silicon precursor and the oxide of hydrogen are first mixed in liquid form to form a liquid mixture. The liquid mixture is then subjected to conditions effective to convert it into a gas which is thereafter fed into the illustrated and preferred hot wall CVD reactor for subsequent deposition processing at temperatures between around 640°C to 900°C. The gaseous mixture is fed into the reactor from a common feed stream.

The above described method can also be employed in cold wall LPCVD systems under the following preferred pressure, temperature and other relevant operating conditions. Cold wall deposition conditions or parameters include pressure conditions of around 10 Torr up to an upper limit of around 80 Torr. A preferred temperature for cold wall processing is around 400°C with rf plasma power at 600W. Further, in accordance with this aspect of the invention, O_2 and He flows respectively, are at 600 sccm and 775 sccm. The preferred organic precursor is TEOS which is delivered by liquid injection at 975 sccm. Additionally, a wafer gap to susceptor is around 230 mils. Under the above conditions, a resulting SiO_2 deposition rate of around 7000 Angstroms/min is possible.

Fig. 4 illustrates schematically a CVD system in which two gas sources or bubblers 30, 32 are shown. Preferably, one of the gas sources contains the organic silicon precursor, preferably TEOS, and the

other gas source contains the additional quantity of the oxide of hydrogen, either of H_2O and/or H_2O_2 . In such system, reactor 18 is separately fed with such gaseous reactants. A preferred concentration of gaseous material provided into reactor 18 comprises less than about 50% by volume of the H_2O and/or H_2O_2 . Even more preferably, the volume of material injected into the reactor comprises between about 5% to 15% by volume of the H_2O and/or H_2O_2 . Quantities of H_2O and H_2O_2 less than about 5% of the volume of material injected into the reactor may be utilized to achieve the above-described advantages. Volumes of about 0.5% or lower of either of the oxides of hydrogen can reduce the decomposition rate of the organic silicon precursor sufficiently to allow CVD depositing of SiO₂ on a silicon substrate.

The above described method is one in which the reactants are provided in separate bubblers or gas sources, and subjected to conditions effective to convert each to a separate gas. Each separate gas is then separately fed into the reactor and exposed to temperature and pressure conditions effective to deposit an SiO₂ layer on the wafers or substrates held therewithin. The gaseous mixtures are fed into the reactor from separate feed streams. As in the first-described method, the above described method may be utilized in cold wall LPCVD systems under conditions which are the same as or similar to those mentioned above.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

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CLAIMS:

1. A semiconductor processing method of chemical vapor depositing SiO₂ on a substrate comprising:

placing a substrate within a chemical vapor deposition reactor;

feeding an organic silicon precursor into the chemical vapor deposition reactor having the substrate positioned therein under conditions effective to decompose the precursor into SiO₂ which deposits on the substrate and into a gaseous oxide of hydrogen; and

feeding an additional quantity of the gaseous oxide of hydrogen into the reactor while feeding the organic silicon precursor into the reactor.

- 2. The semiconductor processing method of claim 1, wherein the organic silicon precursor and the additional quantity of the gaseous oxide of hydrogen are fed into the reactor from separate feed streams.
- 3. The semiconductor processing method of claim 1, wherein the organic silicon precursor and the additional quantity of the gaseous oxide of hydrogen are fed into the reactor from a common feed stream.

4. The semiconductor processing method of claim 1, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the oxide of hydrogen in liquid form to form a liquid mixture;

converting the liquid mixture to a gaseous mixture; and feeding the gaseous mixture into the reactor.

5. The semiconductor processing method of claim 1, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the oxide of hydrogen in liquid form to form a liquid mixture, the quantity of the organic silicon precursor being greater by volume than the quantity of the oxide of hydrogen;

converting the liquid mixture to a gaseous mixture; and feeding the gaseous mixture into the reactor.

6. The semiconductor processing method of claim 1, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the oxide of hydrogen in liquid form to form a liquid mixture, the quantity of the oxide of hydrogen comprising between about 5%-15% of the liquid mixture volume;

converting the liquid mixture to a gaseous mixture; and feeding the gaseous mixture into the reactor.

7. The semiconductor processing method of claim 1, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the oxide of hydrogen in liquid form to form a liquid mixture:

converting the liquid mixture to a gaseous mixture, the converting step including heating the liquid mixture to a temperature of between about 65° C to 80° C; and

feeding the gaseous mixture into the reactor.

8. The semiconductor processing method of claim 1, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the oxide of hydrogen in liquid form to form a liquid mixture, the quantity of the organic silicon precursor being greater by volume than the quantity of the oxide of hydrogen;

converting the liquid mixture to a gaseous mixture, the converting step including heating the liquid mixture to a temperature of between about 65° C to 80° C; and

feeding the gaseous mixture into the reactor.

9. The semiconductor processing method of claim 1, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the oxide of hydrogen in liquid form to form a liquid mixture, the quantity of the oxide of hydrogen comprising between about 5%-15% of the liquid mixture volume;

converting the liquid mixture to a gaseous mixture, the converting step including heating the liquid mixture to a temperature of between about 65° C to 80° C; and

feeding the gaseous mixture into the reactor.

- 10. The semiconductor processing method of claim 1 wherein the organic silicon precursor is selected from the group consisting of silane, tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclotetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).
- 11. The semiconductor processing method of claim 1, wherein the chemical vapor deposition reactor is a hot wall reactor.
- 12. The semiconductor processing method of claim 1, wherein the chemical vapor deposition reactor is a cold wall reactor.
- 13. A semiconductor processing method of reducing the decomposition rate of an organic silicon precursor in a chemical vapor deposition process of depositing SiO_2 on a substrate within a chemical vapor deposition reactor comprising feeding at least one of H_2O and H_2O_2 into the reactor while feeding the organic silicon precursor.
- 14. The semiconductor processing method of claim 13, wherein the at least one of H_2O and H_2O_2 is fed into the reactor separately from the organic silicon precursor.

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- 15. The semiconductor processing method of claim 13, wherein the at least one of H_2O and H_2O_2 is injected into the reactor separately from the organic silicon precursor, and comprises less than about 50% by volume of material injected into the reactor.
- 16. The semiconductor processing method of claim 13, wherein the at least one of H_2O and H_2O_2 is injected into the reactor separately from the organic silicon precursor, and comprises between about 5% to 15% by volume of material injected into the reactor.
- 17. The semiconductor processing method of claim 13, wherein the at least one of H_2O and H_2O_2 is injected into the reactor separately from the organic silicon precursor, and comprises less than about 5% by volume of material injected into the reactor.
- 18. The semiconductor processing method of claim 13, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the at least one of $\rm H_2O$ and $\rm H_2O_2$ in liquid form to form a liquid mixture;

converting the liquid mixture to a gaseous mixture; and feeding the gaseous mixture into the reactor.

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19. The semiconductor processing method of claim 13, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the at least one of H_2O and H_2O_2 in liquid form to form a liquid mixture, the liquid mixture comprising no less than about 0.5% by volume of the at least one of H_2O and H_2O_2 ;

converting the liquid mixture to a gaseous mixture; and feeding the gaseous mixture into the reactor.

20. The semiconductor processing method of claim 13, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the at least one of H_2O and H_2O_2 in liquid form to form a liquid mixture, the liquid mixture comprising between about 5% to 15% by volume of the at least one of H_2O and H_2O_2 ;

converting the liquid mixture to a gaseous mixture; and feeding the gaseous mixture into the reactor.

21. The semiconductor processing method of claim 13, wherein the organic silicon precursor is selected from the group consisting of silane, tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclotetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).

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- 22. The semiconductor processing method of claim 13, wherein the chemical vapor deposition reactor is a hot wall reactor.
- 23. The semiconductor processing method of claim 13, wherein the chemical vapor deposition reactor is a cold wall reactor.
- 24. A semiconductor processing method of chemical vapor depositing SiO₂ on a substrate comprising:

placing a substrate within a chemical vapor deposition reactor; and feeding an organic silicon precursor and feeding an oxide of hydrogen into the chemical vapor deposition reactor having the substrate positioned therein under conditions effective to deposit an SiO₂ layer on the substrate.

25. The semiconductor processing method of claim 24, wherein the feeding steps collectively comprise:

mixing a quantity of the organic silicon precursor in liquid form and a quantity of the oxide of hydrogen in liquid form to form a liquid mixture, the liquid mixture comprising less than about 15% by volume of the oxide of hydrogen;

heating the liquid mixture to a temperature sufficient to produce a gas containing at least some organic silicon precursor and at least some oxide of hydrogen; and

feeding the produced gas into the reactor.

- 26. The semiconductor processing method of claim 24, wherein the volume of material injected into the reactor has no more than about 15% by volume of the oxide of hydrogen.
- 27. The semiconductor processing method of claim 24, wherein the volume of material injected into the reactor has between about 5% to 15% by volume of the oxide of hydrogen.
- 28. The semiconductor processing method of claim 24, wherein the volume of material injected into the reactor has between about 0.5% to 5% by volume of the oxide of hydrogen.

- 29. The semiconductor processing method of claim 24, wherein the organic silicon precursor is selected from the group consisting of: silane, tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclotetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).
- 30. The semiconductor processing method of claim 24, wherein the chemical vapor deposition reactor is a hot wall reactor.
- 31. The semiconductor processing method of claim 24, wherein the chemical vapor deposition reactor is a cold wall reactor.
- 32. A semiconductor processing method of reducing the formation of undesired reaction intermediates in a chemical vapor deposition decomposition reaction of an organic silicon precursor into silicon dioxide within a chemical vapor deposition reactor comprising feeding at least one of H_2O and H_2O_2 into the reactor with the organic silicon precursor.
- 33. The semiconductor processing method of claim 32 wherein the at least one of H_2O and H_2O_2 is fed into the reactor separately from the organic silicon precursor.

- 34. The semiconductor processing method of claim 32 wherein the at least one of H_2O and H_2O_2 is first combined with the organic silicon precursor, and then fed into the reactor with the organic silicon precursor.
- 35. The semiconductor processing method of claim 32, wherein the organic silicon precursor is selected from the group consisting of: silane, tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclotetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).
- 36. The semiconductor processing method of claim 32, wherein the chemical vapor deposition reactor is a hot wall reactor.
- 37. The semiconductor processing method of claim 32, wherein the chemical vapor deposition reactor is a cold hot reactor.

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38. A semiconductor processing method of chemical vapor depositing SiO₂ on a substrate comprising:

placing a substrate within a chemical vapor deposition reactor;

mixing a quantity of an organic silicon precursor in liquid form and a quantity of an oxide of hydrogen in liquid form to form a liquid mixture, the organic silicon precursor being selected from the group consisting of: silane, tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclo-tetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS), the oxide of hydrogen being selected from the group consisting of: H_2O and H_2O_2 , the quantity of the oxide of hydrogen comprising between about 5%-15% of the liquid mixture volume;

converting the liquid mixture to a gaseous mixture by heating the liquid mixture to a temperature of between about 65℃ to 80℃; and feeding the gaseous mixture into the reactor.

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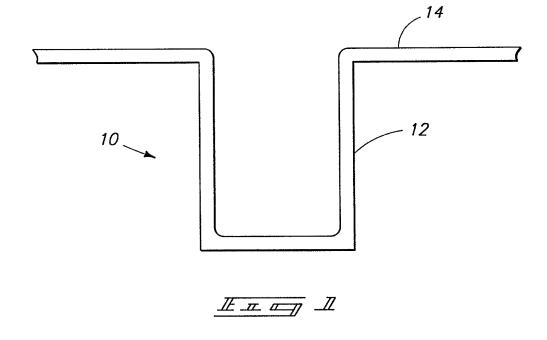
23

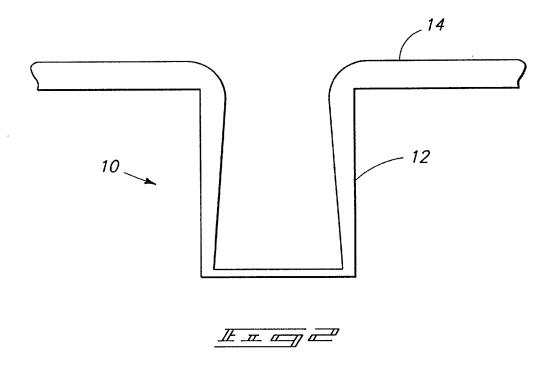
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ABSTRACT OF THE DISCLOSURE

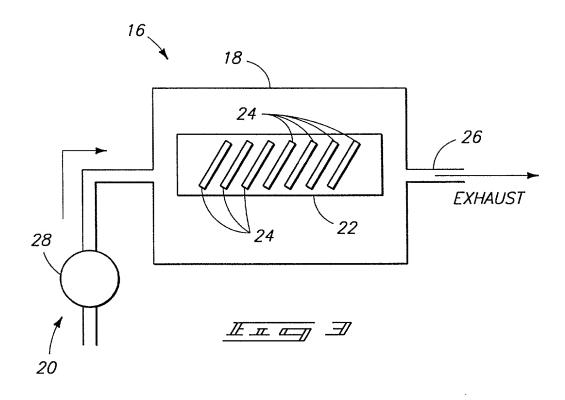
The invention provides semiconductor processing methods of depositing SiO₂ on a substrate. In a preferred aspect, the invention provides methods of reducing the formation of undesired reaction intermediates in a chemical vapor deposition (CVD) decomposition reaction. In one implementation, the method is performed by feeding at least one of H₂O and H₂O₂ into a reactor with an organic silicon precursor. For example, in one exemplary implementation, such components are, in gaseous form, fed separately into the reactor. another exemplary implementation, such components are combined in liquid form prior to introduction into the reactor, and thereafter rendered into a gaseous form for provision into the reactor. The invention can be practiced with or in both hot wall and cold wall CVD systems.

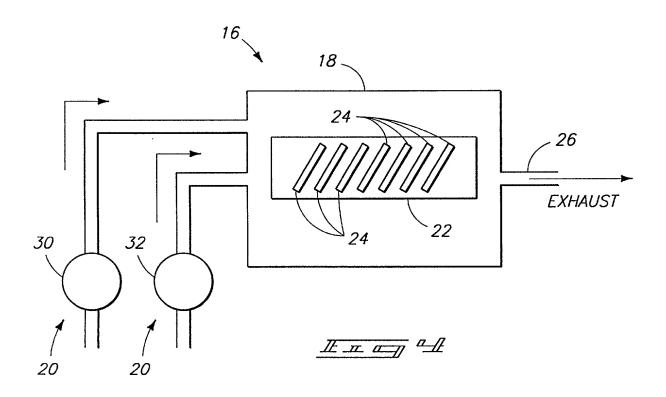
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DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Semiconductor Processing Methods Of Chemical Vapor Depositing SiO₂ On A Substrate, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

POWER OF ATTORNEY:

As a named Inventor, I hereby appoint the following attorneys and agent to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory, Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

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